WHAT IS CLAIMED IS

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1. A semiconductor device comprising:

a semiconductor chip having electrodes;

an insulation layer formed on a surface of the semiconductor chip where the electrodes of the semiconductor chip are formed; and

a wiring layer formed on the insulation layer,

the electrodes of the semiconductor chip and the wiring layer being connected to each other via connection members disposed in the insulation layer.

2. The semiconductor device according to claim 1, wherein

the connection members include wire bumps disposed on the electrodes of the semiconductor chip.

3. The semiconductor device according to claim 2, wherein

the connection members further include cured conductive pastes formed on the wire bumps.

4. The semiconductor device according to claim 1, wherein

the connection members include a metal layer formed on the electrodes of the semiconductor chip, and cured conductive pastes disposed on the metal layer.

5. The semiconductor device according to claim 1, further comprising

a solder resist layer having openings, for covering the wiring layer,

solder balls disposed in the openings of the solder resist layer, connected to the wiring layer.

6. The semiconductor device according to claim 1, wherein

an additional insulation layer is formed on a surface of the semiconductor chip, which is opposite to the surface of the

semiconductor chip where the electrodes are formed.

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7. A method for fabricating a semiconductor device comprising the steps of:

preparing a wafer including a plurality of semiconductor chips with electrodes formed on;

forming connection members on the electrodes of the respective semiconductor chips;

forming an insulation layer in a thickness to cover the connection members on the surfaces of the respective semiconductor chips where the electrodes of the semiconductor chips are formed;

polishing the insulation layer to expose the connection members;

forming an electroless plated layer on the insulation layer; and

forming, with the electroless plated layer as a feeder layer of electric current, an electrolytic plated layer on the electroless plated layer selectively only in regions for a wiring layer;

etching off the electroless plated layer except regions of the electroless plated layer corresponding to the electrolytic plated layer to form the wiring layer including the electroless plated layer and the electrolytic plated layer; and

severing the wafer into the respective semiconductor chips to fabricate the semiconductor device.

8. The method for fabricating a semiconductor device according to claim 7, further comprising the steps of:

forming a solder resist layer having openings on the wiring layer; and

forming solder balls in the openings of the solder resist layer, connected to the wiring layer.

9. The method for fabricating a semiconductor device according to claim 7, wherein

the connection members are formed by forming wire bumps on the electrodes of the semiconductor chips by wire bonding.

10. The method for fabricating a semiconductor device according to claim 9, wherein

the connection members are formed by forming cured conductive pastes on the wire bumps.

11. The method for fabricating a semiconductor device according to claim 7, wherein

the connection members are formed on the electrodes of the semiconductor chips by forming a metal layer by sputtering and forming cured conductive pastes on the metal layer.

12. The method for fabricating a semiconductor device according to claim 7, wherein

in the step of forming an electrolytic plated layer, a resist pattern of a prescribed configuration is formed on the electroless plated layer, and the electrolytic plated layer is selectively formed with the resist pattern as a plating- resistant mask.

13. The method for fabricating a semiconductor device according to claim 12, wherein

in the step of forming an wiring layer by etching, the resist pattern of a prescribed configuration on the electroless plated layer removed, and then the exposed electroless plated layer is removed by soft etching without damaging the wiring layer.

14. The method for fabricating a semiconductor device according to claim 7, wherein

the step of polishing the insulation layer is followed by surface roughening processing for roughening the surface of the insulation layer.

15. The method for fabricating a semiconductor device according to claim 8, wherein

in the step of forming a solder resist layer, a photosensitive solder resist is formed by screen printing, to cover the wiring layer, and prescribed regions of the photosensitive solder resist are exposed and developed to form the openings so as to expose the wiring layer.

add A3